V61C51164096
256K X 16 HIGH SPEED STATIC RAM

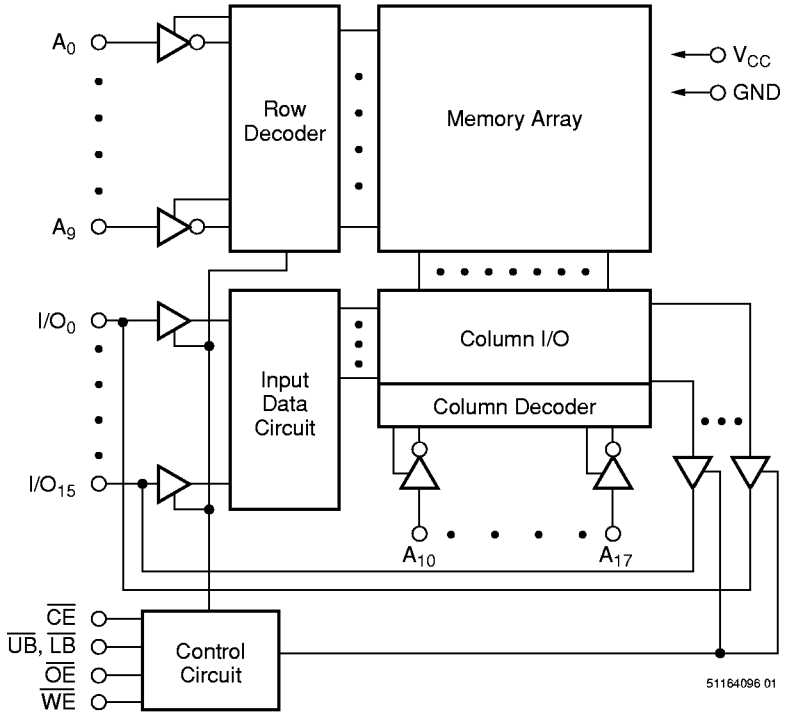
Features

- High-speed: 15, 20, 25 ns
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Low data retention current (V_{CC} = 2V)
- Single 5V ± 10% Power Supply
- Low CMOS Standby current of 10 mA max
- Packages
  - 44-pin TSOP
  - 44-pin 400 mil SOJ

Description

The V61C51164096 is a 4,194,304-bit static random-access memory organized as 262,144 words by 16 bits. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The V61C51164096 is available in 44-pin SOJ, and 44-pin TSOP.

Functional Block Diagram



Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)			Temperature Mark
	T	R	15	20	25	
0°C to 70°C	•	•	•	•	•	Blank

Pin Descriptions

A_0–A_{17} Address Inputs
These 17 address inputs select one of the 256K x 16 bit segments in the RAM.

$\overline{CE}$ Chip Enable Inputs
$\overline{CE}$ is active LOW. $\overline{CE}$ enables must be active to read from or write to the device. If chip enable is not active, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when deselected.

$\overline{OE}$ Output Enable Input
The Output Enable input is active LOW. When $\overline{OE}$ is LOW with $\overline{CE}$ LOW and $\overline{WE}$ HIGH, data of the selected memory location will be available on the I/O pins. When $\overline{OE}$ is HIGH, the I/O pins will be in the high impedance state.

$\overline{WE}$ Write Enable Input
An active LOW input, $\overline{WE}$ input controls read and write operations. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, the data present on the I/O pins will be written into the selected memory location.

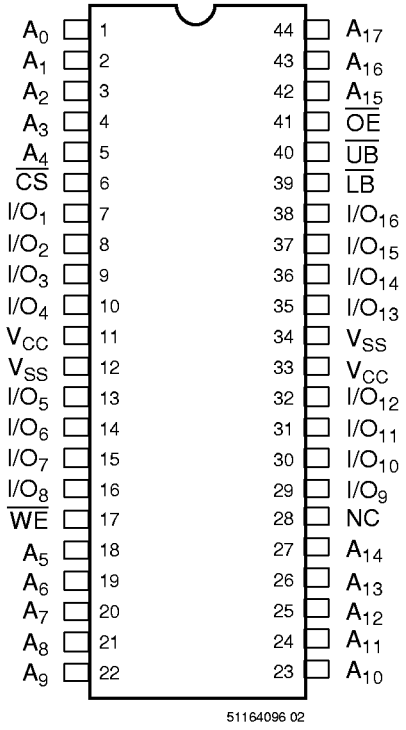
I/O_0–I/O_{15} Data Input and Data Output Ports
These 8 bidirectional ports are used to read data from and write data into the RAM.

V_{CC} Power Supply

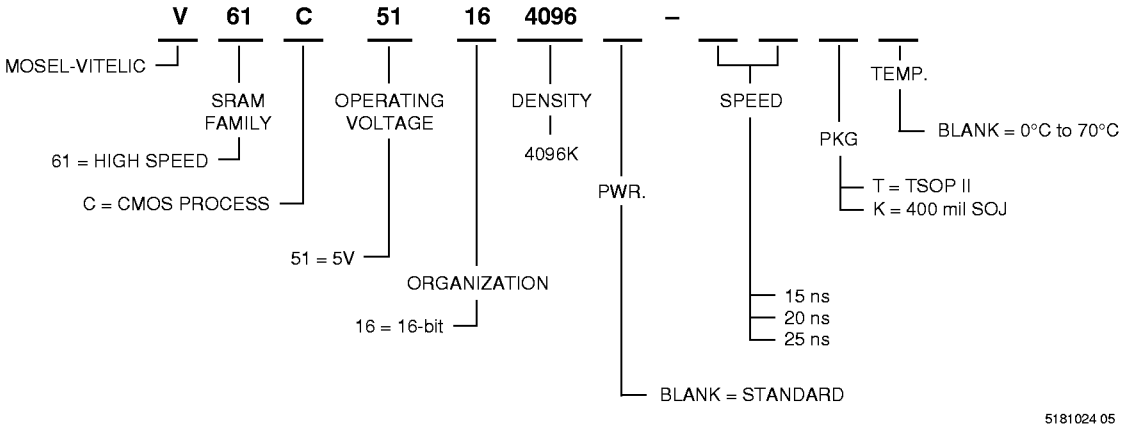
GND Ground

Pin Configurations (Top View)

44-Pin SOJ/TSOP



Ordering Information



Absolute Maximum Ratings (1)

Symbol	Parameter	Commercial	Units
V_{CC}	Supply Voltage	-0.5 to +7	V
V_N	Input Voltage	-0.5 to +7	V
V_{DQ}	Input/Output Voltage Applied	V_{CC} + 0.5	V
T_{BIAS}	Temperature Under Bias	-10 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C

NOTE:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance*

T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	8	pF

NOTE:

1. This parameter is guaranteed by design and not tested.

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O Pin I/O_1-I/O_8	I/O Pin I/O_9-I/O_{16}
Not Select	H	X	X	X	X	High Z	High Z
Output Disable	L	H	H	X	X	High Z	High Z
	L	X	X	H	H		
Read	L	H	L	L	H	D_{OUT}	High Z
				H	L	High Z	D_{OUT}
				L	L	D_{OUT}	D_{OUT}
Write	L	L	X	L	H	D_{IN}	High Z
				H	L	High Z	D_{IN}
				L	L	D_{IN}	D_{IN}

NOTE:

X = Don't Care, L = LOW, H = HIGH

DC Electrical Characteristics (over all temperature ranges, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input LOW Voltage(1,2)		-0.5	—	0.8	V
V_{IH}	Input HIGH Voltage(1)		2.2	—	6	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}	-2	—	2	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{CE}_1$ = V_{IH}, V_{OUT} = 0V to V_{CC}	-2	—	2	µA
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 2.1mA	—	—	0.4	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = -1mA	2.4	—	—	V

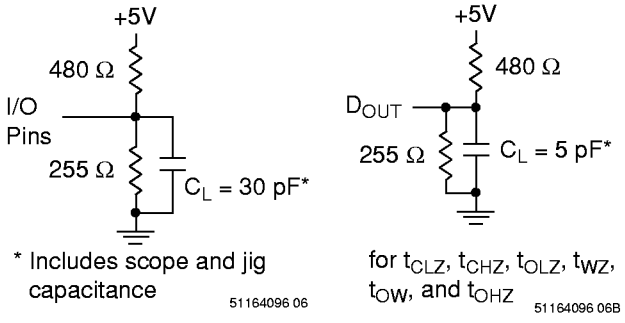
Symbol	Parameter	Min.	Max.	Units
I_{CC1}	Average Operating Current, $\overline{CE}_1$ = V_{IL}, CE_2 = V_{IH}, Output Open, V_{CC} = Max., f = f_{MAX}(3)	—	210	mA
I_{SB}	TTL Standby Current $\overline{CE}_1 \geq V_{IH}$, $CE_2 \leq V_{IL}$, V_{CC} = Max.	—	50	mA
I_{SB1}	CMOS Standby Current, $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, V_{CC} = Max.	—	10	mA

NOTES:
1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. V_{IL} (Min.) = -2.0V for pulse width < 10ns.
3. $f_{MAX} = 1/t_{RC}$.
4. Maximum values.

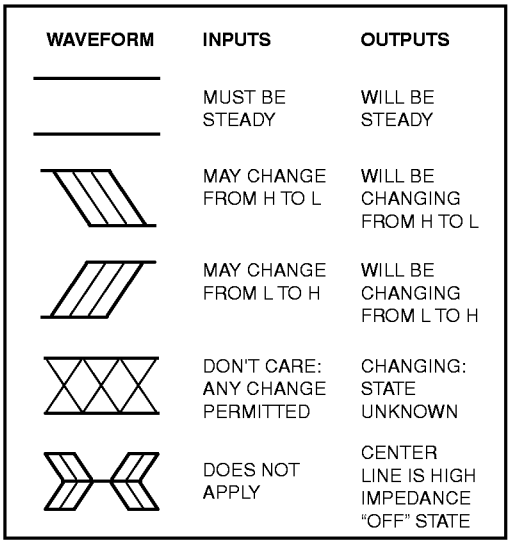
AC Test Conditions

Input Pulse Levels	0 to 3V
Input Rise and Fall Times	3 ns
Timing Reference Levels	1.5V
Output Load	see below

AC Test Loads and Waveforms



Key to Switching Waveforms

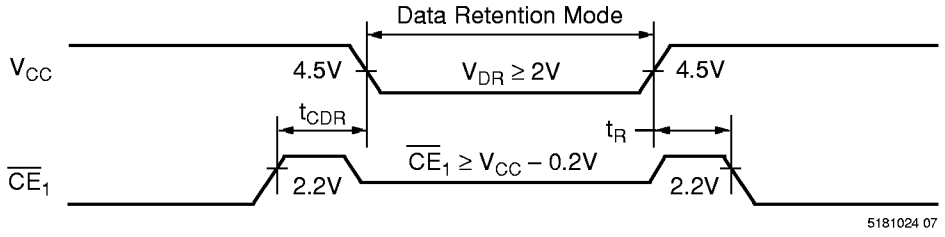


Data Retention Characteristics

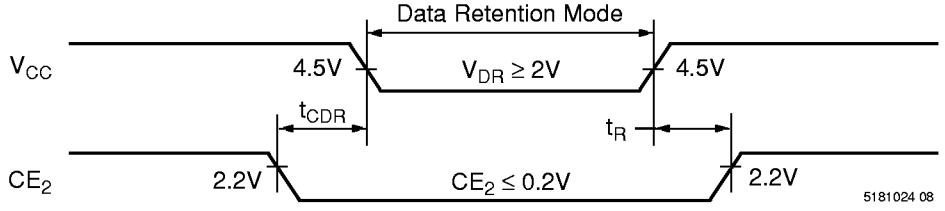
Symbol	Parameter	Min.	Typ.(2)	Max.	Units
V_{DR}	V_{CC} for Data Retention $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, or $V_{IN} \leq 0.2V$	2.0	—	5.5	V
I_{CCDR}	Data Retention Current $\overline{CE}_1 \geq V_{DR} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, or $V_{IN} \leq 0.2V$	—	—	150	µA
t_{CDR}	Chip Deselect to Data Retention Time	0	—	—	ns
t_R	Operation Recovery Time (see Retention Waveform)	t_{RC}(1)	—	—	ns

NOTES:
1. t_{RC} = Read Cycle Time
2. T_A = +25°C.

Low V_{CC} Data Retention Waveform (1) ($\overline{CE}_1$ Controlled)



Low V_{CC} Data Retention Waveform (2) (CE_2 Controlled)



AC Electrical Characteristics

(over all temperature ranges)

Read Cycle

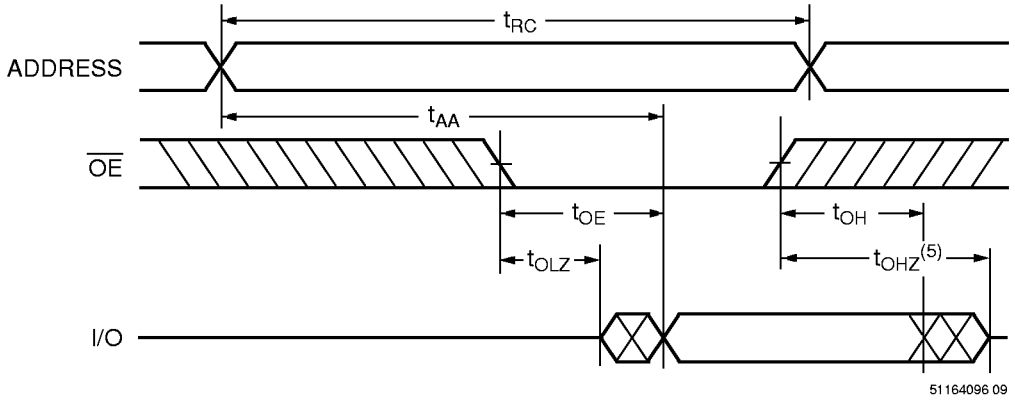
Parameter Name	Parameter	-15		-20		-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	ns
t_{ACS}	Chip Enable Access Time	—	15	—	20	—	25	ns
t_{BA}	$\overline{UB}$, $\overline{LB}$ Access Time	—	7	—	9	—	10	ns
t_{OE}	Output Enable to Output Valid	—	7	—	9	—	10	ns
t_{CLZ}	Chip Enable to Output in Low Z	3	—	3	—	3	—	ns
t_{BLZ}	$\overline{UB}$, $\overline{LB}$ Enable to Output in Low Z	0	—	0	—	0	—	ns
t_{OLZ}	Output Enable to Output in Low Z	0	—	0	—	0	—	ns
t_{CHZ}	Chip Disable to Output in High Z	0	7	0	9	0	10	ns
t_{OHZ}	Output Disable to Output in High-Z	0	7	0	9	0	10	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{BHZ}	$\overline{UB}$, $\overline{LB}$ Disable to Output in High-Z	0	7	—	9	—	10	ns

Write Cycle

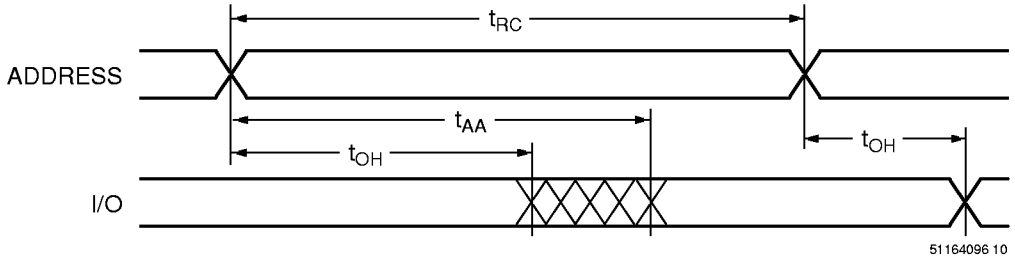
Parameter Name	Parameter	-15		-20		-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	15	—	20	—	25	—	ns
t_{CW}	Chip Enable to End of Write	12	—	14	—	15	—	ns
t_{BW}	$\overline{UB}$, $\overline{LB}$ Valid to Write End	12	—	14	—	15	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	12	—	14	—	15	—	ns
t_{WP}	Write Pulse Width	12	—	14	—	15	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}	Write to Output High-Z	0	7	0	9	0	10	ns
t_{WLZ}	Write to Output Low Z	3	—	3	—	5	—	ns
t_{DW}	Data Setup to End of Write	8	—	10	—	11	—	ns
t_{DH}	Data Hold from End of Write	0	—	0	—	0	—	ns
t_{OW}	Write End to Output in Low-Z	3	—	3	—	3	—	ns

Switching Waveforms (Read Cycle)

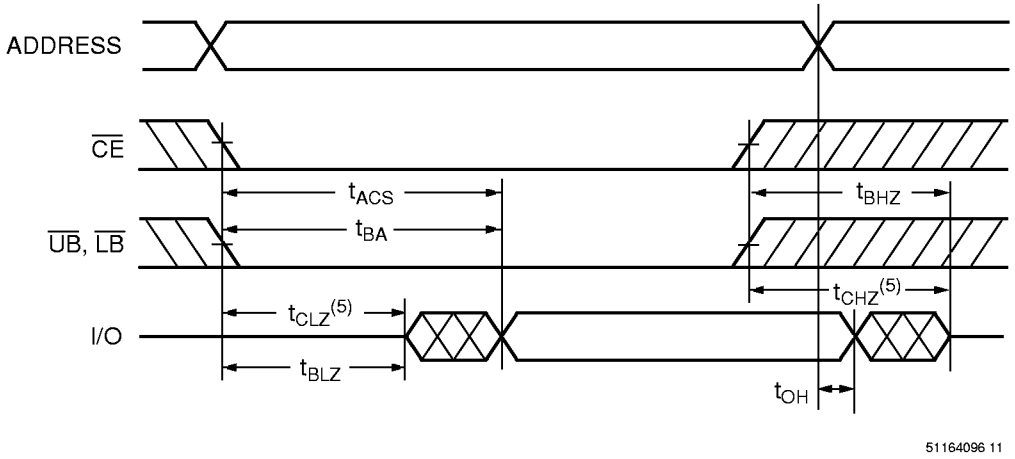
Read Cycle 1[1, 2]



Read Cycle 2[1, 2, 4]



Read Cycle 3[1, 3, 4]

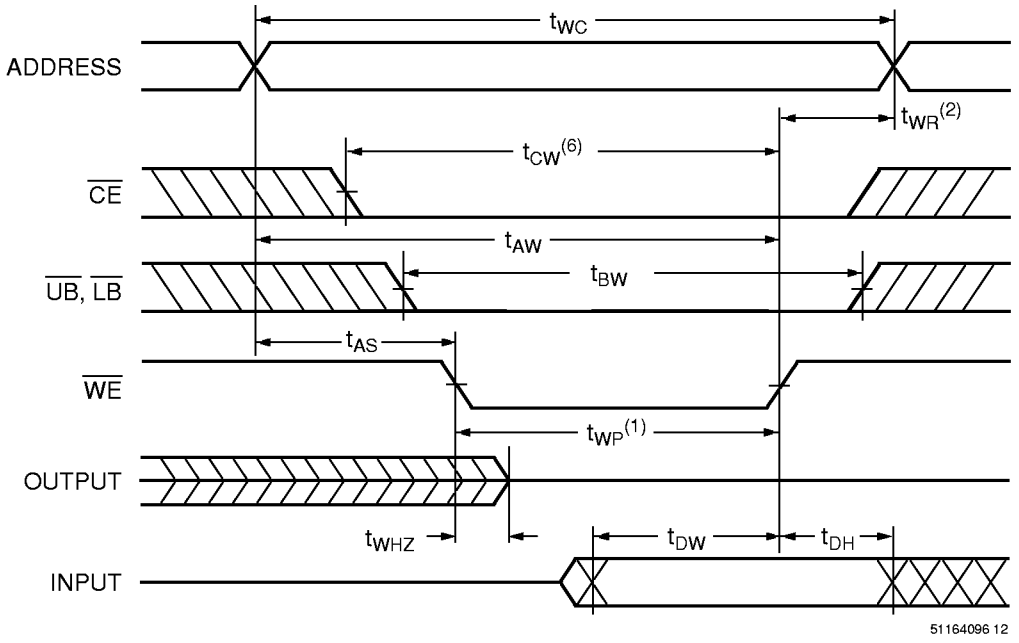


NOTES:

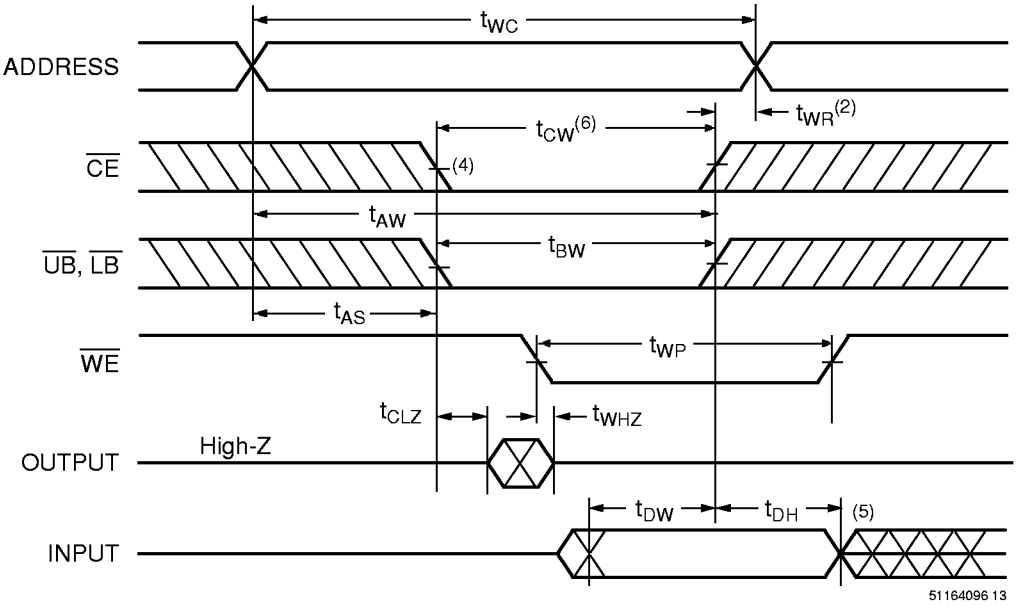
1. $\overline{WE}$ = V_{IH}.
2. $\overline{CE}_1$ = V_{IL} and CE_2 = V_{IH}.
3. Address valid prior to or coincident with $\overline{CE}_1$ transition LOW and/or CE_2 transition HIGH.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state with C_L = 5pF. This parameter is guaranteed and not 100% tested.

Switching Waveforms (Write Cycle)

Write Cycle 1 ($\overline{WE}$ Controlled)(4)



Write Cycle 2 (CE Controlled)(4)

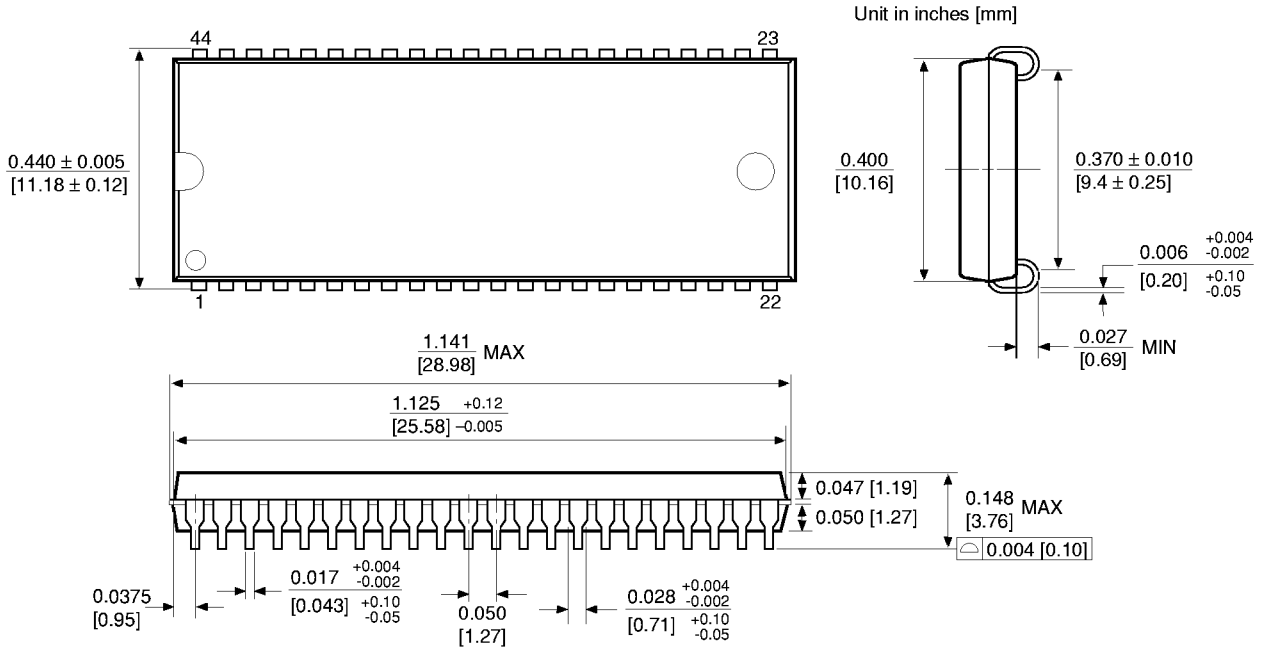


NOTES:

1. The internal write time of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All signals must be active to initiate and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
2. t_{WR} is measured from the earlier of $\overline{CE}$.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. $\overline{OE}$ = V_{IL} or V_{IH}. However it is recommended to keep $\overline{OE}$ at V_{IH} during write cycle to avoid bus contention.
5. If $\overline{CE}$ is LOW, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. t_{CW} is measured from $\overline{CE}$ going low.

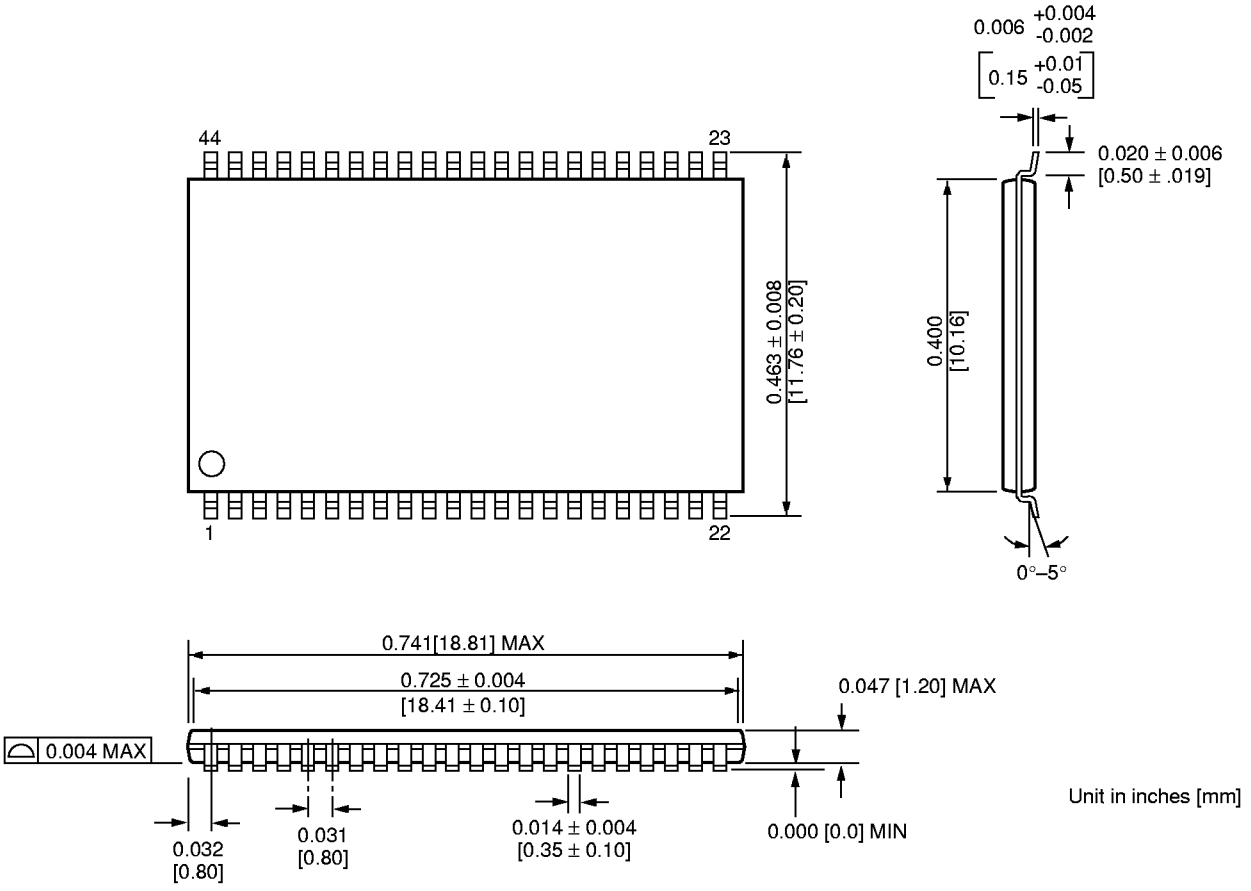
Package Diagrams

44-Pin 400 mil SOJ



Package Diagrams

44-Pin 400 mil TSOP



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